**Amendments to the Claims**

This listing of claims will replace all prior versions, and listings, of claims in the application, in which deleted matter is shown using ~~strikethrough~~ and added matter is underlined:

**Listing of Claims:**

1. (Previously presented) A multiple channel programmable gamma correction voltage generator, comprising:

a reference voltage applied across a resistor ladder;

said resistor ladder including M adjustable tap resistors distributed along said resistor ladder, each providing a corresponding one of M tap voltages distributed according to a gamma correction value, wherein M is a positive integer;

said resistor ladder comprising a plurality of first resistors coupled in series, each of said plurality of first resistors comprising a plurality of second resistors coupled in series forming a plurality of intermediate locations;

M buffers, each having an input receiving a corresponding one of said M tap voltages and an output providing a corresponding one of M gamma correction voltages;

select logic which inserts each of said M adjustable tap resistors into said resistor ladder into M of said plurality of first resistors by inserting a corresponding one of said M adjust adjustable tap resistors at a selected one of said plurality of intermediate locations of a corresponding one of said plurality of first resistors, and that selects a tap point of each of said M adjustable tap resistors to select each of said M tap voltages based on corresponding select values; and

a programmable non-volatile memory device, coupled to said select logic, that provides said select values indicative of said gamma correction value.

2. (Original) The multiple channel programmable gamma correction voltage generator of claim 1, wherein:

each of said M adjustable tap resistors comprises P resistors coupled in series forming P-1 intermediate junctions, wherein P is a positive integer; and

wherein said select logic comprises P-1 switches, each having a first terminal coupled to a corresponding one of said P-1 intermediate junctions and a second terminal coupled to a common tap node providing a corresponding one of said M tap voltages.

3. (Original) The multiple channel programmable gamma correction voltage generator of claim 2, wherein said select logic includes decoder logic which closes one of said P-1 switches of each of said M adjustable tap resistors to select each of said M tap voltages based on a corresponding one of M select values from said memory device.

4. (Original) The multiple channel programmable gamma correction voltage generator of claim 3, wherein said decoder logic comprises M decoders, each receiving a corresponding one of said M select values and selecting a corresponding one of said P-1 switches of a corresponding one of said M adjustable tap resistors.

5. (Previously presented) The multiple channel programmable gamma correction voltage generator of claim 1, wherein:

said plurality of first resistors includes M+1 first resistors evenly distributed along said resistor ladder forming M intermediate locations;

wherein at least M of said first resistors each comprise Q second resistors coupled in series forming Q-1 intermediate locations and an end location, wherein Q is a positive integer;

wherein said select logic comprises Q switch sets, each coupled between a respective pair of said second resistors at a corresponding one of said Q intermediate locations and said end location; and

wherein each of said switch sets is operative, when selected, to decouple said Q second resistors at a corresponding one of said Q-1 intermediate locations and said end location and to insert a corresponding one of said M adjustable tap resistors.

6. (Original) The multiple channel programmable gamma correction voltage generator of claim 5, further comprising:

each of said M adjustable tap resistors comprising P third resistors coupled in series forming P-1 intermediate junctions, wherein P is a positive integer; and

said select logic comprising P-1 switches, each having a first terminal coupled to a corresponding one of said P-1 intermediate junctions and a second terminal coupled to a common tap node providing a corresponding one of said M tap voltages.

7. (Original) The multiple channel programmable gamma correction voltage generator of claim 6, wherein said memory device asserts first signals to select from among said switch sets of each said first resistor for gross adjustment and asserts second signals to select from among said switches of each of said M adjustable tap resistors for fine adjustment.

8. (Original) The multiple channel programmable gamma correction voltage generator of claim 6, wherein said select logic comprises decoder logic which provides a set of M gross adjustment values and provides a set of M fine adjustment values to select each of said M tap voltages based on a corresponding one of said M select values, wherein each said gross adjustment value selects a corresponding one of said switch sets, and wherein each fine adjustment value selects a corresponding one of said switches.

9. (Original) The multiple channel programmable gamma correction voltage generator of claim 1, further comprising a set of latches with an external load coupled to said memory device and providing said select values to said select logic.

10. (Original) The multiple channel programmable gamma correction voltage generator of claim 9, wherein said memory device stores a plurality of sets of select values, each corresponding to a different gamma correction value, and wherein said memory device includes an address control input for selecting from among said plurality of sets of select values and loading said set of latches.

11. (Original) The multiple channel programmable gamma correction voltage generator of claim 1, wherein said resistor ladder is incorporated into a single integrated circuit (IC).

12. (Original) The multiple channel programmable gamma correction voltage generator of claim 11, wherein said buffers, select logic and memory device are incorporated into said IC.

13. (Original) The multiple channel programmable gamma correction voltage generator of claim 1, wherein each of said M buffers comprises an operational amplifier configured as a voltage follower.

14. (Previously presented) An integrated circuit (IC), comprising:

a resistor ladder coupled to a reference voltage;

a plurality of adjustable tap resistors distributed along said resistor ladder and providing a plurality of selectable tap voltages;

a plurality of first resistors distributed along said resistor ladder, each coupled to a corresponding one of said plurality of adjustable tap resistors, each first resistor comprising:

a plurality of second resistors coupled in series forming a plurality of first junctions; and

first switch logic that inserts said corresponding one of said plurality of adjustable tap resistors at one of said plurality of first junctions;

a programmable non-volatile memory that stores at least one digital gamma value;

select logic, coupled to said memory, to said first switch logic and to said plurality of adjustable tap resistors, that controls said first switch logic and that selects each of said selectable tap voltages according to said at least one digital gamma value; and

a plurality of buffers having inputs receiving selected tap voltages and outputs that provide a plurality of gamma correction voltages.

15. (Original) The IC of claim 14, wherein each of said plurality of adjustable tap resistors comprises:

a plurality of resistors coupled in series and forming a plurality of junctions; and

switch logic that selects one of said plurality of junctions.

16. Canceled.

17. (Previously presented) The IC of claim 14, wherein:

each of said plurality of adjustable tap resistors comprises:

a plurality of third resistors coupled in series and forming a plurality of second junctions; and

second switch logic that selects one of said plurality of second junctions; and

said select logic providing a gross adjustment to each said first switch logic and a fine adjustment to each said second switch logic.

18. (Original) The IC of claim 14, further comprising:

a set of latches, coupled to said memory, that enables programming and selection of a plurality of a plurality of digital gamma values in said memory; and

control logic providing address control to said memory for selecting one of said plurality of digital gamma values.

19. (Previously presented) An imaging system, comprising:

an imaging device having a gamma factor;

a driver circuit that provides a set of DC reference voltages to said imaging device based on a set of gamma corrected bias voltages; and

a programmable gamma correction voltage generator that provides said set of gamma corrected bias voltages configured to compensate for said gamma factor, said programmable gamma correction voltage generator comprising:

a reference voltage coupled across a resistor ladder comprising a plurality of resistors coupled in series and forming a plurality of intermediate junctions;

a plurality of potentiometers distributed along said resistor ladder and providing a plurality of variable tap voltages, wherein each of said plurality of potentiometers is inserted at a corresponding one of said plurality of intermediate junctions;

a programmable non-volatile memory that stores at least one digital gamma value;

select logic, coupled to said memory and to said plurality of potentiometers, that selects from among said plurality of intermediate junctions for inserting said plurality of potentiometers and that selects each of said variable tap voltages according to said digital gamma value; and

a plurality of buffers having inputs receiving selected tap voltages and outputs that provide said set of gamma corrected bias voltages.

20. (Original) The imaging system of claim 19, wherein said programmable gamma correction voltage generator is incorporated on an IC.

21. (Original) The imaging system of claim 19, wherein said imaging device comprises an LCD panel.

22. (Original) The imaging system of claim 19, further comprising control logic coupled to said memory via address control, wherein said control logic enables selection of a plurality of digital gamma values stored in said memory.